CLAIMS

We Claim:

1. A circuit arrangement for regulating the duty cycle of an electrical signal, the circuit arrangement comprising:

-a first input differential amplifier including two transistors, to which a first input signal is applied,

-a first current source for controlling a first current through the first input differential amplifier,

-a second input differential amplifier including two transistors, to which the first input signal is applied,

-a second current source for controlling a second current through the second input differential amplifier,

-means for generating a fluctuating voltage signal in response to the first and second currents,

-a buffer device for converting the fluctuating voltage signal into a digital output signal, and for transmitting the digital output signal to an output terminal,

-a capacitance, and

-means for charging and discharging the capacitance in synchronization with the digital output signal,

-wherein a voltage present at the capacitance is fed to the first and second current sources as a control voltage such that regulation of the two current sources is effected in opposite senses.

2. The circuit arrangement as claimed in claim 1, wherein the first input differential amplifier comprises two n-channel FET transistors, and the first current source is connected between ground and source terminals of the transistors of the first input differential amplifier.

3. The circuit arrangement as claimed in claim 1, wherein the second input differential amplifier comprises two p-channel FET transistors, and the second current source is connected between an operating voltage and source terminals

of the transistors of the second input differential amplifier.

4. The circuit arrangement as claimed in claim 1, wherein the means for charging and discharging the capacitance comprises a charge pump with a first current source for charging the capacitance, and a second current source for discharging the capacitance, and wherein one of the first and second current sources is activated in response to the presence of a high digital output signal and the other of the two current sources is activated in response to the presence of a low digital output signal, thereby respectively charging and discharging the capacitance.

5. The circuit arrangement as claimed in claim 1, wherein the means for generating the fluctuating voltage signal from the first and second currents is formed by first and second current mirror circuits, the first and second current mirror circuits respectively comprising a first current mirror transistor and a second current mirror transistor connected in series, wherein the fluctuating voltage signal is tapped off between the first and second current mirror transistors.

6. The circuit arrangement as claimed in claim 5, wherein each of the first and second current mirror circuits comprises:

-a first transistor, which is identical to one of the transistors of the respective input differential amplifier,

-a current mirror comprising a first current mirror transistor and a second current mirror transistor with a reference current and a control current,

-the reference current of the current mirror being formed by the current generated by the first transistor,

-the first transistor and the first current mirror transistor being connected in series and

-wherein the second current mirror transistor of the two current mirrors being connected to one another and the voltage signal whose level fluctuates being tapped off between these transistors.

7. The circuit arrangement as claimed in claim 1, further comprising an output stage providing a current output.

8. The circuit arrangement as claimed in claim 1, further comprising an output stage providing a voltage output.

9. The circuit arrangement as claimed in claim 1, wherein the individual transistors are embodied in one of CMOS technology, as bipolar transistors, and embodied in BiCMOS technology.

10. A circuit arrangement for regulating the duty cycle of an electrical signal, the circuit arrangement comprising:

a first current source for generating a first current;

a first differential amplifier for passing the first current along a first branch when the electrical signal has a first voltage value;

a first current mirror circuit including a first current mirror transistor having a gate terminal connected to the first branch of the first differential amplifier;

a second current source for generating a second current;

a second differential amplifier for passing the second current along a second branch when the electrical signal has a second voltage value;

a second current mirror circuit including a second current mirror transistor connected in series with the first current transistor, wherein the second current mirror transistor has a gate terminal connected to the second branch of the second differential amplifier;

a buffer device for converting a fluctuating voltage signal generated between the first and second current mirror transistors into a digital output signal, and for transmitting the digital output signal to an output terminal;

a capacitor; and

means for charging and discharging the capacitor in synchronization with the digital output signal,

wherein a control voltage generated across the capacitor is fed to the first and second current sources, and

wherein the first and second current sources respectively regulate the first and second currents in response to the control signal such that a duty cycle of the digital output signal is set to a predetermined value.

11. The circuit arrangement as claimed in claim 10,

wherein the first current source is connected between the first differential amplifier and ground, and

wherein the second current source is connected between an operating voltage source and the second differential amplifier.

12. The circuit arrangement as claimed in claim 11,

wherein the first differential amplifier comprises first and second n-channel transistors having source terminals connected to the first current source, the first n-channel transistor having a gate terminal connected to receive an inverted electrical signal, and the second n-channel transistor having a gate terminal connected to receive the electrical signal and a drain terminal connected to the first branch, and

wherein the second differential amplifier comprises first and second p-channel transistors having drain terminals connected to ground, the first p-channel transistor having a gate terminal connected to receive the electrical signal and a source terminal connected to the second branch, and the

second p-channel transistor having a gate terminal connected to receive the inverted electrical signal.

13. The circuit arrangement as claimed in claim 12, further comprising:

third and fourth p-channel transistors respectively connected in series with the first and second n-channel transistors between the operating voltage source and the first current source, wherein a gate terminal of the third p-channel transistor is connected to a drain terminal of the first n-channel transistor, and a gate terminal of the fourth p-channel transistor is connected to a drain terminal of the second n-channel transistor and to the gate terminal of the first current mirror transistor; and

third and fourth n-channel transistors respectively connected in series with the first and second p-channel transistors, the third and fourth n-channel transistors having source terminals connected to ground, wherein a gate terminal of the third n-channel transistor is connected to a drain terminal of the first p-channel transistor and to the gate terminal of the second current mirror transistor, and a gate terminal of the fourth n-channel transistor is connected to a drain terminal of the second p-channel transistor.

14. The circuit arrangement as claimed in claim 13,

wherein the first current mirror transistor comprises a p-channel transistor, and wherein the second current mirror transistor comprises an n-channel transistor.

15. The circuit arrangement as claimed in claim 10, wherein the means for charging and discharging the capacitor comprises:

a first current source connected between the system voltage source and a first terminal of the capacitor;

a second current source connected in parallel with the capacitor and having a terminal connected to ground; and

means for controlling the first and second current sources such that the first current source is activated and the second current source is deactivated when the digital output signal has a first voltage value, thereby charging the capacitor, and such that the first current source is deactivated and the second current source is activated when the digital output signal has a second voltage value, thereby discharging the capacitor.

16. A circuit arrangement for regulating the duty cycle of an electrical signal, the circuit arrangement comprising:

a first current source for generating a first current in response to a control voltage;

a first differential amplifier connected to the first current source such that the first current source is connected between the first differential amplifier and ground, wherein the first differential amplifier includes an n-channel transistor for passing the first current when the electrical signal has a first voltage value;

a second current source for generating a second current in response to the control voltage;

a second differential amplifier connected to the second current source such that the second current source is connected between the second differential amplifier and an operating voltage source, wherein the second differential amplifier includes a p-channel transistor for passing the second current when the electrical signal has a first voltage value;

a p-channel current mirror transistor having a source connected to the operating voltage source, and a gate terminal connected to a drain terminal of the n-channel transistor;

an n-channel current mirror transistor having a source connected to ground, a gate terminal connected to a drain terminal of the p-channel transistor, and a drain terminal connected to a drain terminal of the p-channel current mirror

transistor;

means for generating a digital output signal in response to a fluctuating voltage signal generated at the drain terminals of the n-channel and p-channel current mirror transistors, and

means for generating the control signal applied to the first and second current sources in response to the digital output signal such that the first and second current sources respectively regulate the first and second currents in a manner that sets a duty cycle of the digital output signal to a predetermined value.